DS26C31T/DS26C31M CMOS Quad TRI-STATE® Differential Line Driver

Check for Samples: DS26C31M, DS26C31T

FEATURES

- **TTL input compatible**
- **Typical propagation delays: 6 ns**
- **Typical output skew: 0.5 ns**
- **Outputs will not load line when V_{CC} = 0V**
- **DS26C31T meets the requirements of EIA standard RS-422**
- **Operation from single 5V supply**
- **TRI-STATE outputs for connection to system buses**
- **Low quiescent current**
- **Available in surface mount**
- **Mil-Std-883C compliant**

DESCRIPTION

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (1). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Connection Diagram

Dual-In-Line Package

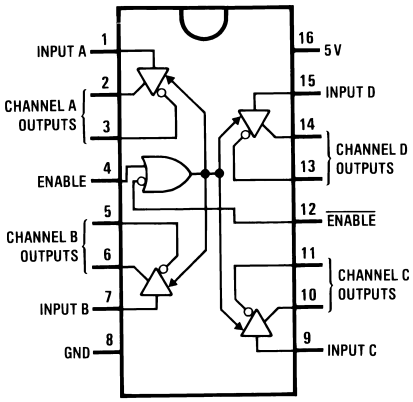


Figure 1. Top View
Order Number DS26C31TM or DS26C31TN
See NS Package Number M16A or N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

(1) The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

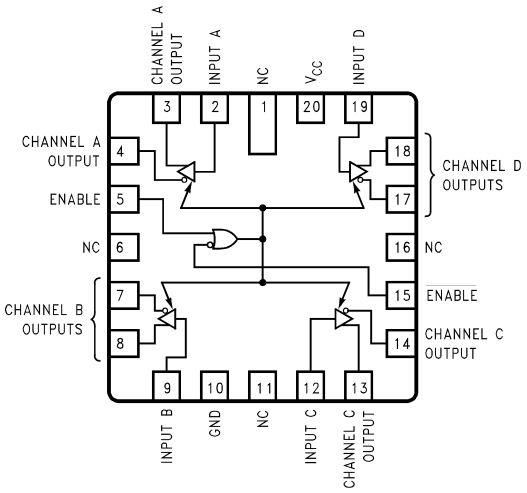


Figure 2. 20-Lead Ceramic Leadless Chip Carrier (E)

Truth Table(1)

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting	Inverting
			Output	Output
L	H	X	Z	Z
All other		L	L	H
combinations of		H	H	L
enable inputs				

(1) L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE (high impedance)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current,	
per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max. Power Dissipation (P_D) @25°C (3)	
Ceramic “J” Pkg.	2419 mW
Plastic “N” Pkg.	1736 mW
SOIC “M” Pkg.	1226 mW
Ceramic “W” Pkg.	1182 mW
Ceramic “E” Pkg.	2134 mW
Lead Temperature (T_L)	
(Soldering, 4 sec.)	260°C
This device does not meet 2000V ESD Rating. (4)	

(1) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.
(2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of “Electrical Characteristics” provide conditions for actual device operation.
(3) Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.
(4) ESD Rating: HBM (1.5 kΩ, 100 pF); Inputs ≥ 1500V; Outputs ≥ 1000V; EIAJ (0Ω, 200 pF) ≥ 350V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS26C31T	−40	+85	°C
DS26C31M	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ± 10% (unless otherwise specified) (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL},		2.5	3.4		V
		I_{OUT} = −20 mA					
V_{OL}	Low Level Output	$V_{IN} = V_{IH}$ or V_{IL},			0.3	0.5	V
	Voltage	I_{OUT} = 20 mA					
V_T	Differential Output	R_L = 100Ω		2.0	3.1		V
	Voltage	(2)					
$\|V_T\| - \|\overline{V_T}\|$	Difference In	R_L = 100Ω				0.4	V
	Differential Output	(2)					
V_{OS}	Common Mode	R_L = 100Ω			1.8	3.0	V
	Output Voltage	(2)					
$\|V_{OS} - \overline{V_{OS}}\|$	Difference In	R_L = 100Ω				0.4	V
	Common Mode Output	(2)					
I_{IN}	Input Current	$V_{IN} = V_{CC}$, GND, V_{IH}, or V_{IL}				±1.0	µA
I_{CC}	Quiescent Supply	DS26C31T	$V_{IN} = V_{CC}$ or GND		200	500	µA
	Current (3)	I_{OUT} = 0 µA	V_{IN} = 2.4V or 0.5V		0.8	2.0	mA
			(3)				
		DS26C31M	$V_{IN} = V_{CC}$ or GND		200	500	µA
		I_{OUT} = 0 µA	V_{IN} = 2.4V or 0.5V		0.8	2.1	mA
			(3)				
I_{OZ}	TRI-STATE Output	$V_{OUT} = V_{CC}$ or GND					
	Leakage Current	ENABLE = V_{IL}			±0.5	±5.0	µA
		$\overline{\text{ENABLE}}$ = V_{IH}					
I_{SC}	Output Short	$V_{IN} = V_{CC}$ or GND		−30		−150	mA
	Circuit Current	(2) (4)					
I_{OFF}	Output Leakage Current	DS26C31T	V_{OUT} = 6V			100	µA
	Power Off (2)	V_{CC} = 0V	V_{OUT} = −0.25V			−100	µA
		DS26C31M	V_{OUT} = 6V			100	µA
		V_{CC} = 0V	V_{OUT} = 0V			−100	µA
			(5)				

(1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) See EIA Specification RS-422 for exact test conditions.
(3) Measured per input. All other inputs at V_{CC} or GND.
(4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.
(5) The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

Switching Characteristics

V_{CC} = 5V ±10%, $t_r \le 6$ ns, $t_f \le 6$ ns (Figure 3, Figure 4, Figure 5, Figure 6) (1)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t_{PLH}, t_{PHL}	Propagation Delays	S1 Open	2	6	11	14	ns
	Input to Output						
Skew	(2)	S1 Open		0.5	2.0	3.0	ns
t_{TLH}, t_{THL}	Differential Output Rise	S1 Open		6	10	14	ns
	And Fall Times						
t_{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t_{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t_{PHZ}	Output Disable Time	S1 Closed		5	9	12	ns
	(3)						
t_{PLZ}	Output Disable Time	S1 Closed		7	11	14	ns
	(3)						
C_{PD}	Power Dissipation			50			pF
	Capacitance (4)						
C_{IN}	Input Capacitance			6			pF

(1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
(4) C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

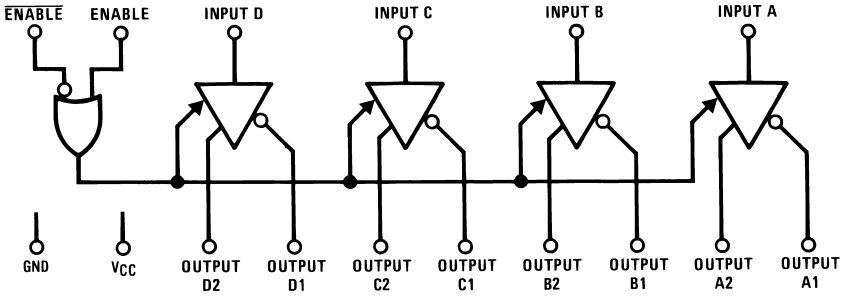
Comparison Table of Switching Characteristics into "LS-Type" Load

V_{CC} = 5V, T_A = 25°C, $t_r \le 6$ ns, $t_f \le 6$ ns (Figure 4, Figure 6, Figure 7, Figure 8) (1)

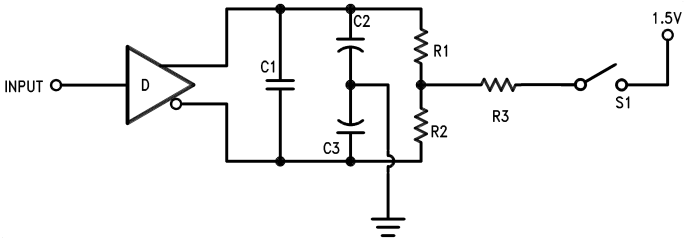
Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delays	C_L = 30 pF					
	Input to Output	S1 Closed	6	8	10	15	ns
		S2 Closed					
Skew	(2)	C_L = 30 pF					
		S1 Closed	0.5	1.0	2.0	6.0	ns
		S2 Closed					
t_{THL}, t_{TLH}	Differential Output Rise	C_L = 30 pF					
	and Fall Times	S1 Closed	4	6			ns
		S2 Closed					
t_{PLZ}	Output Disable Time	C_L = 10 pF					
	(3)	S1 Closed	6	9	15	35	ns
		S2 Open					
t_{PHZ}	Output Disable Time	C_L = 10 pF					
	(3)	S1 Open	4	7	15	25	ns
		S2 Closed					
t_{PZL}	Output Enable Time	C_L = 30 pF					
		S1 Closed	14	20	20	30	ns
		S2 Open					
t_{PZH}	Output Enable Time	C_L = 30 pF					
		S1 Open	11	17	20	30	ns
		S2 Closed					

(1) This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.
(2) Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
(3) Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Logic Diagram



AC Test Circuit and Switching Time Waveforms



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

Figure 3. AC Test Circuit

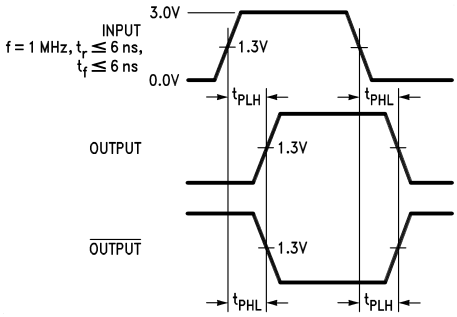


Figure 4. Propagation Delays

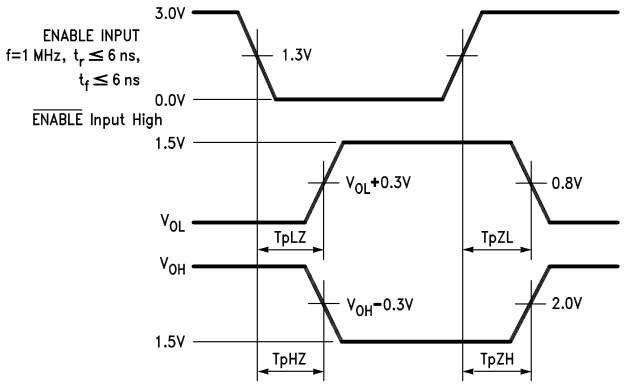
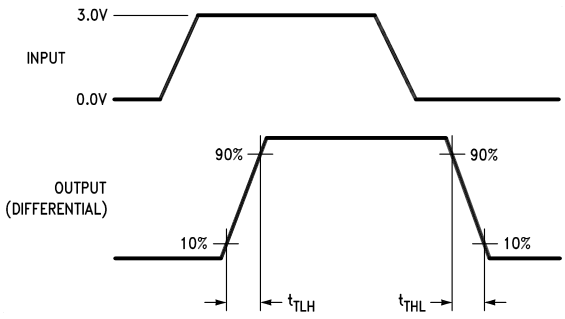


Figure 5. Enable and Disable Times



Input pulse; f = 1 MHz, 50%; $t_r \leq$ 6 ns, $t_f \leq$ 6 ns

Figure 6. Differential Rise and Fall Times

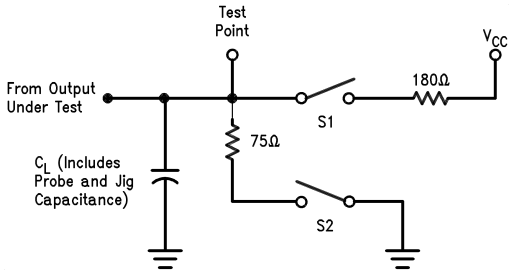


Figure 7. Load AC Test Circuit for "LS-Type" Load

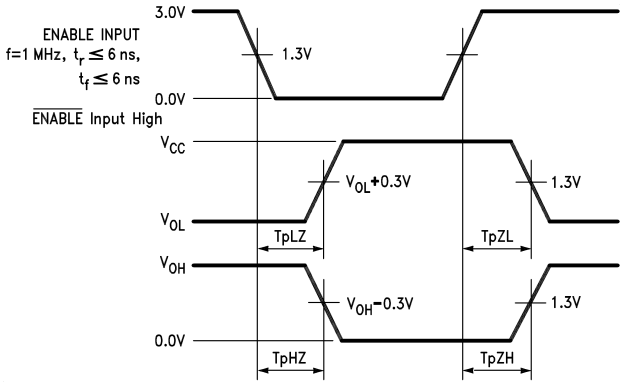
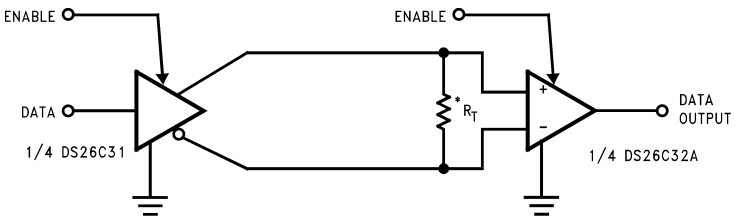


Figure 8. Enable and Disable Times for "LS-Type" Load

Typical Applications

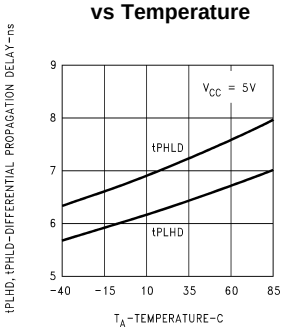


*R_T is optional although highly recommended to reduce reflection.

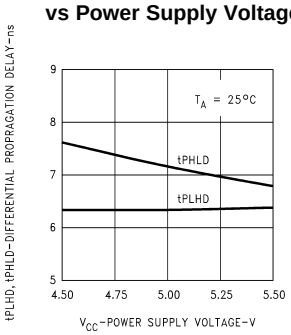
Figure 9. Two-Wire Balanced System, RS-422

Typical Performance Characteristics

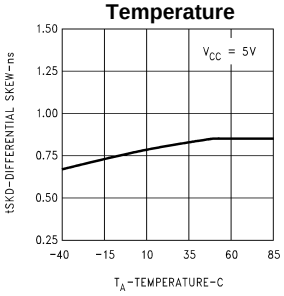
Differential Propagation Delay vs Temperature



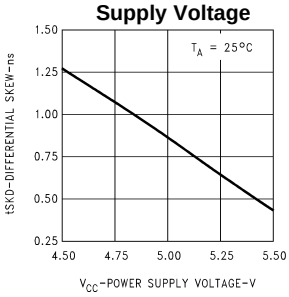
Differential Propagation Delay vs Power Supply Voltage



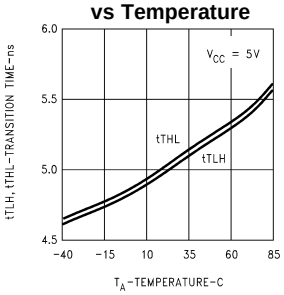
Differential Skew vs Temperature



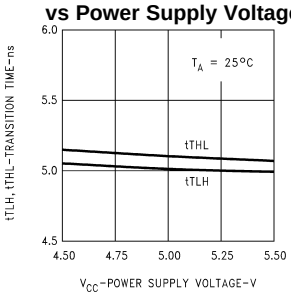
Differential Skew vs Power Supply Voltage



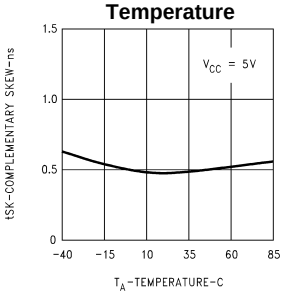
Differential Transition Time vs Temperature



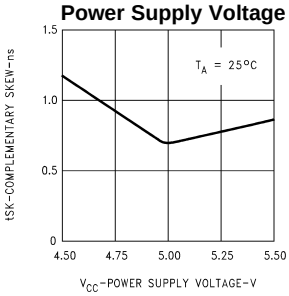
Differential Transition Time vs Power Supply Voltage



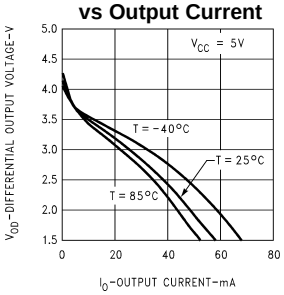
Complementary Skew vs Temperature



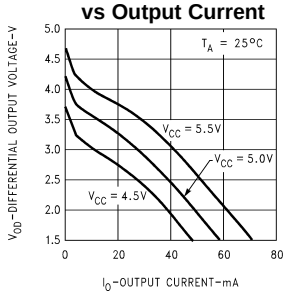
Complementary Skew vs Power Supply Voltage



Differential Output Voltage vs Output Current

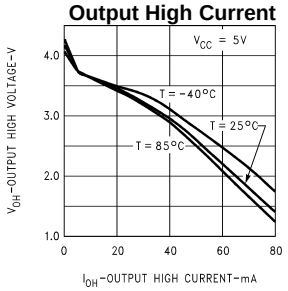


Differential Output Voltage vs Output Current

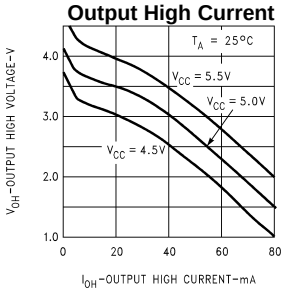


Typical Performance Characteristics (continued)

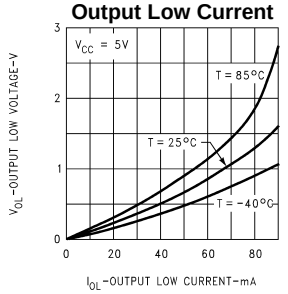
Output High Voltage vs Output High Current



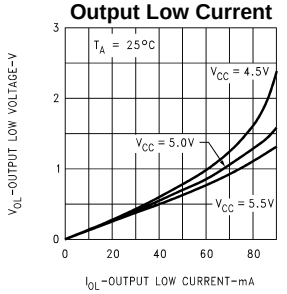
Output High Voltage vs Output High Current



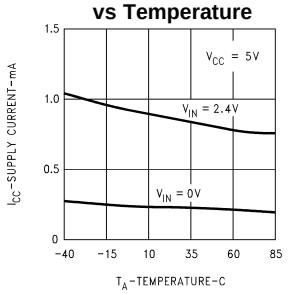
Output Low Voltage vs Output Low Current



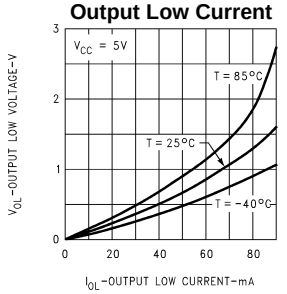
Output Low Voltage vs Output Low Current



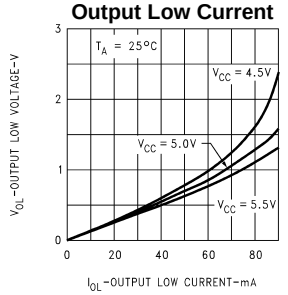
Supply Current vs Temperature



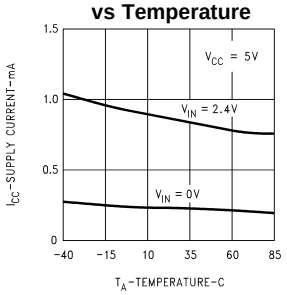
Output Low Voltage vs Output Low Current



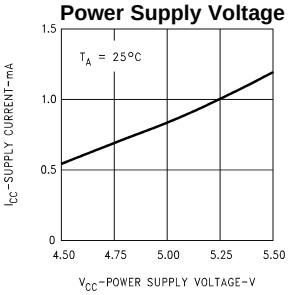
Output Low Voltage vs Output Low Current



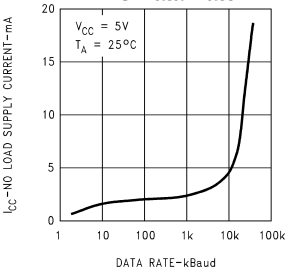
Supply Current vs Temperature



Supply Current vs Power Supply Voltage

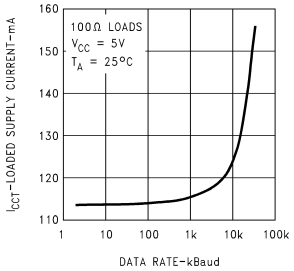


No Load Supply Current vs Data Rate

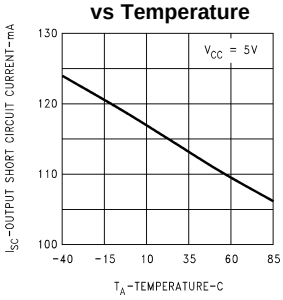


Typical Performance Characteristics (continued)

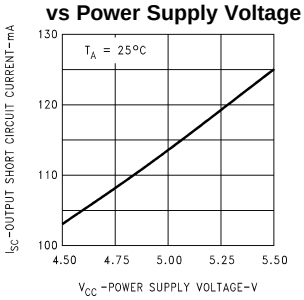
Loaded Supply Current vs Data Rate



Output Short Circuit Current vs Temperature



Output Short Circuit Current vs Power Supply Voltage



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DS26C31TM	ACTIVE	SOIC	D	16	48	TBD	CU SNPB	Level-1-235C-UNLIM	
DS26C31TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
DS26C31TMX	ACTIVE	SOIC	D	16	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
DS26C31TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
DS26C31TN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Level-1-NA-UNLIM	
DS26C31TN/NOPB	ACTIVE	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	

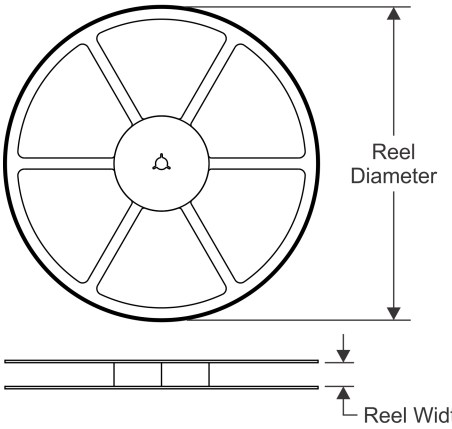
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

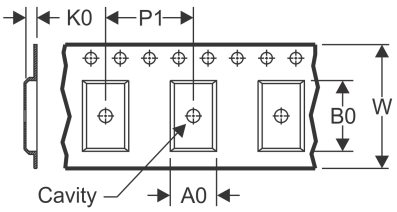
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

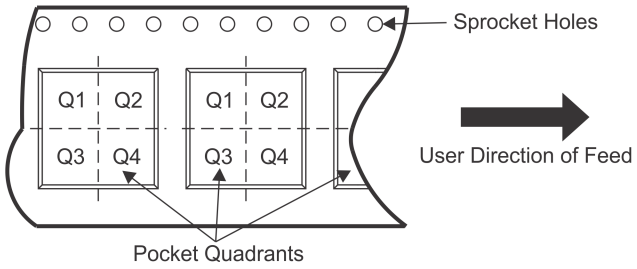


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

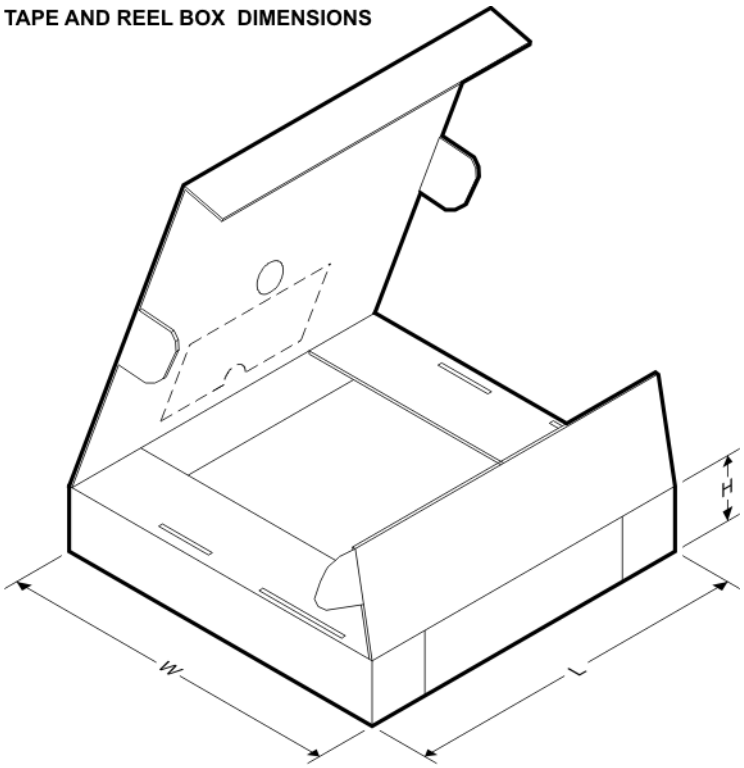
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C31TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26C31TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

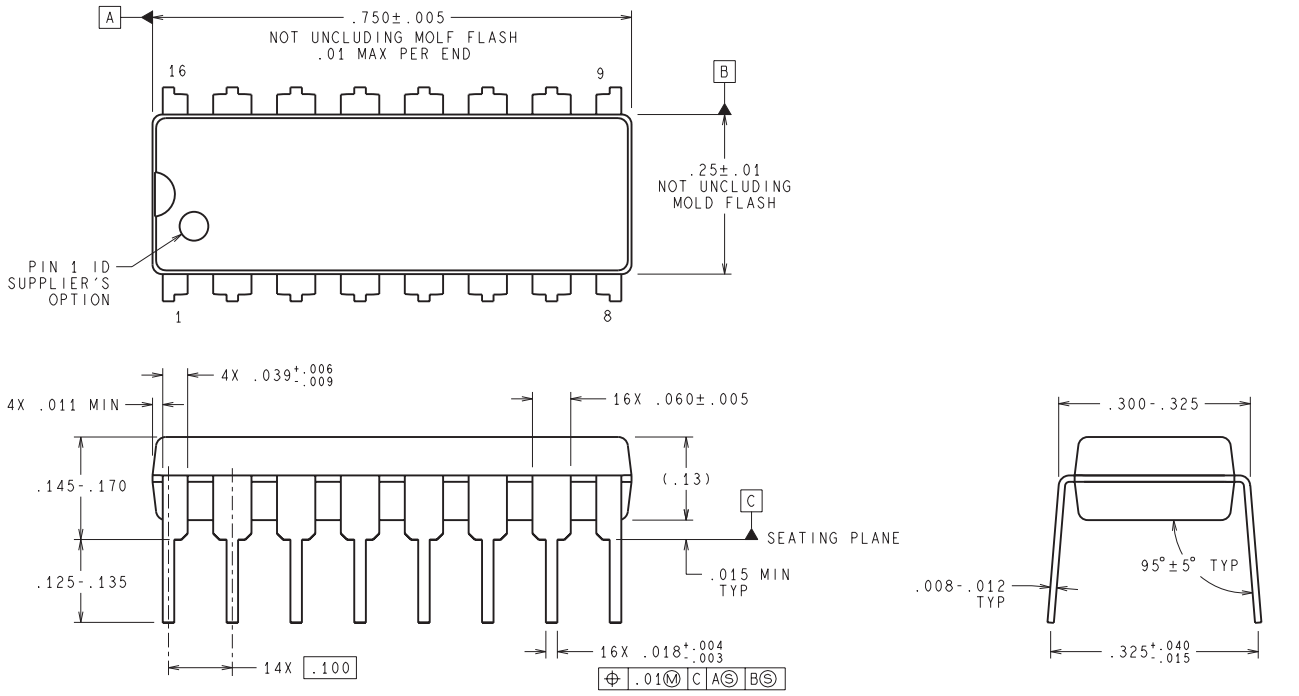
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26C31TMX	SOIC	D	16	2500	349.0	337.0	45.0
DS26C31TMX/NOPB	SOIC	D	16	2500	349.0	337.0	45.0

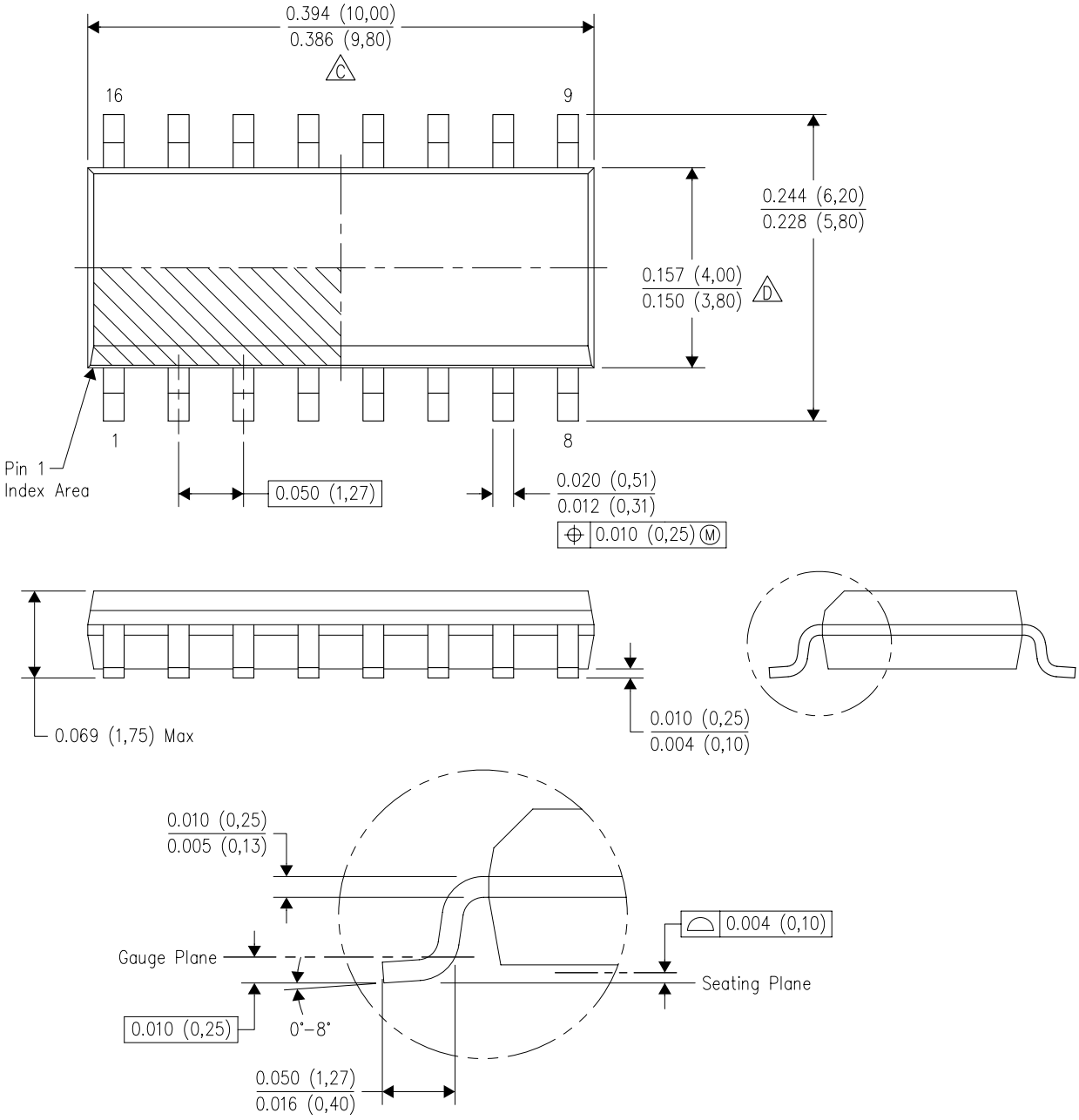
NFG0016E



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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